

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re Patent Application of:

Hongyong ZHANG et al.

Serial No. 09/190,618

Filed: November 12, 1998

For: SEMICONDUCTOR DEVICE AND  
METHOD FOR FABRICATING THE  
SAME

) Group Art Unit:

) Examiner:

) CERTIFICATE OF MAILING  
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Adelle M. Stamp

RESPONSE

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

The Official Action mailed August 19, 2003, has been received and its contents carefully noted. Filed concurrently herewith is a *Request for a One Extension of Time*, which extends the shortened statutory period for response to December 19, 2003. Accordingly, the Applicants respectfully submit that this response is being timely filed.

The Applicants note with appreciation the consideration of the Information Disclosure Statements filed on November 12, 1998, December 17, 1998, October 10, 2000, January 3, 2001, March 12, 2001, August 24, 2001, September 24, 2001, May 13, 2002, November 6, 2002, and July 23, 2003. A further Information Disclosure Statement is submitted herewith and careful review and consideration of this IDS is requested.

Claims 1-25, 34-39, 41 and 42 are pending in the present application, of which claims 1, 6, 11, 16, 19, 37 and 42 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance.

Paragraph 3 of the Official Action rejects claims 1-4, 6-9, 12-14, 16-22, 24, 25, 34-38, 41 and 42 as obvious based on the combination of U.S. Patent No. 5,323,042 to Matsumoto and U.S. Patent No. 5,412,493 to Kunii et al. The Applicants respectfully

submit that a *prima facie* case of obviousness cannot be maintained against the independent claims of the present invention.

The prior art, either alone or in combination, does not teach or suggest all the features of the independent claims. The independent claims of the present invention recite that a distance between edges of the channel forming region and edges of the pair of first regions of the first thin film transistor is greater than that of the second thin film transistor. Matsumoto and Kunii do not teach or suggest at least this feature of the present invention.

The Official Action asserts that "by increasing the length of the low level impurity region in the matrix panel TFT [of Kunii], the length of the low level impurity region in the matrix panel TFT will be greater than the low level impurity region in the driving circuit of Matsumoto" (page 6, Paper No. 43). The Applicants respectfully disagree and traverse the above assertion. The Official Action still has not responded to the Applicants' arguments that Matsumoto and Kunii do not teach or suggest any relation between a length of a low level impurity region of a first TFT of an active matrix circuit and that of a second TFT in a driver circuit; that even if Kunii teaches that the length of the low level impurity region should be increased, Kunii fails to disclose or suggest that such length should be increased to some length greater than that of a second TFT in a driver circuit; and that Matsumoto does not disclose the length of the low impurity regions, thus it is impossible to draw any comparison between the LDD regions of Matsumoto and Kunii (see pages 2-3, *Amendment* filed May 23, 2003). Therefore, the Applicants respectfully submit that Matsumoto and Kunii, either alone or in combination, do not teach or suggest all the features of the present invention.

Since Matsumoto and Kunii do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) are in order and respectfully requested.

Paragraphs 4-6 of the Official Action reject claims 5, 10, 11, 15, 23 and 39 as obvious based on the combination of Matsumoto, Kunii and either U.S. Patent No. 5,028,551 to Dohjo et al., U.S. Patent No. 5,430,320 to Lee, or JP 56-40269 to Iizuka. Either Dohjo, Lee or Iizuka does not cure the deficiencies in Matsumoto and Kunii.


As noted in the *Amendment* filed May 23, 2003, the Official Action relies on Dohjo, Lee and Iizuka to allegedly teach features which are not related to a distance between edges of the channel forming region and edges of the pair of first regions of the first thin film transistor is greater than that of the second thin film transistor. Matsumoto, Kunii and either Dohjo, Lee or Iizuka, either alone or in combination, do not teach or suggest either a distance between edges of the channel forming region and edges of the pair of first regions of the first thin film transistor is greater than that of the second thin film transistor, or any relation between a length of a low level impurity region of a first TFT of an active matrix circuit and that of a second TFT in a driver circuit.

Also, Dohjo, Lee or Iizuka do not teach or suggest any relation between a length of a low level impurity region of a first TFT of an active matrix circuit and that of a second TFT in a driver circuit; that a length of a low level impurity region should be increased to some length greater than that of a second TFT in a driver circuit; or that one should draw comparisons between the LDD regions of two devices.

Since Matsumoto, Kunii and either Dohjo, Lee or Iizuka do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,

  
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